What is claimed is:

1. A clock generation circuit comprising:

first to Nth inversion circuits in which an output of each previous-stage Kth ($1 \leqq K \leqq N-1$) inversion circuit is connected to an input of the corresponding next-stage (K+1)th inversion circuit and an output of the Nth inversion circuit is connected by a feedback line to an input of the first inversion circuit; and

first to Nth buffer circuits having inputs connected to outputs of the first to Nth inversion circuits,

wherein the first to Nth inversion circuits are disposed along a first line that is parallel to the feedback line; and

wherein the first to Nth buffer circuits are disposed along a second line that is parallel to the feedback line but different from the first line.

2. The clock generation circuit as defined in claim 1,

wherein the feedback line is disposed in a region between a region in which the first to Nth inversion circuits are disposed and a region in which the first to Nth buffer circuits are disposed.

3. The clock generation circuit as defined in claim 1, wherein:

the first to Nth inversion circuits are differential-output type inversion circuits;

the first to Nth buffer circuits are differential-input type buffer circuits to which are input differential outputs from the first to Nth inversion circuits;

the feedback line includes a feedback line pair connected to a differential output of the Nth inversion circuit; and

the feedback line pair is disposed in a region between a region in which the first to Nth inversion circuits are disposed and a region in which the first to Nth buffer circuits are disposed.

4. The clock generation circuit as defined in claim 1,

wherein first to (N-1)th dummy lines are connected to the corresponding outputs of the first to (N-1)th inversion circuits and each of the first to (N-1)th dummy lines has parasitic capacitance equal to the parasitic capacitance of the feedback line connected to the output of the Nth inversion circuit.

5. The clock generation circuit as defined in claim 4,

wherein the feedback line and the first to (N-1)th dummy lines are disposed in a region between a region in which the first to Nth inversion circuits are disposed and a region in which the first to Nth buffer circuits are disposed.

6. The clock generation circuit as defined in claim 4, wherein:

the first to Nth inversion circuits are differential-

output type inversion circuits;

the first to Nth buffer circuits are differential-input type buffer circuits to which are input differential outputs from the first to Nth inversion circuits;

the feedback line includes a feedback line pair connected to a differential output of the Nth inversion circuit; and

the first to (N-1)th dummy lines include first to (N-1)th dummy line pairs connected to differential outputs of the first to (N-1)th inversion circuits; and

the feedback line pair and the first to (N-1)th dummy line pairs are disposed in a region between a region in which the first to Nth inversion circuits are disposed and a region in which the first to Nth buffer circuits are disposed.

7. A clock generation circuit comprising:

first to Nth inversion circuits in which an output of each previous-stage Kth ($1 \leqq K \leqq N-1$) inversion circuit is connected to an input of the corresponding next-stage (K+1)th inversion circuit and an output of the Nth inversion circuit is connected by a feedback line to an input of the first inversion circuit; and

first to Nth buffer circuits having inputs connected to outputs of the first to Nth inversion circuits,

wherein first to (N-1)th dummy lines are connected to the corresponding outputs of the first to (N-1)th inversion circuits and each of the first to (N-1)th dummy lines has parasitic capacitance equal to the parasitic capacitance of the

feedback line connected to the output of the Nth inversion circuit.

8. The clock generation circuit as defined in claim 1, further comprising:

an edge detection circuit which detects between which two edges of first to Nth clocks a data edge is located, the first to Nth clocks being obtained on the basis of outputs of the first to Nth buffer circuits; and

a clock selection circuit which selects one of the first to Nth clocks, based on edge detection information from the edge detection circuit, and outputs the selected clock as a sampling clock for sampling data.

9. The clock generation circuit as defined in claim 7, further comprising:

an edge detection circuit which detects between which two edges of first to Nth clocks a data edge is located, the first to Nth clocks being obtained on the basis of outputs of the first to Nth buffer circuits; and

a clock selection circuit which selects one of the first to Nth clocks, based on edge detection information from the edge detection circuit, and outputs the selected clock as a sampling clock for sampling data.

10. The clock generation circuit as defined in claim 8, wherein lines for the first to Nth clocks are disposed

in such a manner that the parasitic capacitances of the lines for the first to Nth clocks are equal.

11. The clock generation circuit as defined in claim 9, wherein lines for the first to Nth clocks are disposed in such a manner that the parasitic capacitances of the lines for the first to Nth clocks are equal.

12. The clock generation circuit as defined in claim 8, wherein:

the edge detection circuit has a first holding circuit which holds data by using a first clock, ... a Jth holding circuit which holds data by using a Jth clock (where: $1 < J < N$), ... and an Nth holding circuit which holds data by using an Nth clock;

the first to Nth holding circuits are disposed along a line parallel to the lines of the first to Nth clocks;

the lines of the first to Nth clocks are connected to inputs of the first to Nth holding circuits, after being looped back in the opposite direction at first to Nth loop-back points; and

the first to Nth loop-back points are provided at positions such that the parasite capacitances of the lines of the first to Nth clocks are equal.

13. The clock generation circuit as defined in claim 9, wherein:

the edge detection circuit has a first holding circuit

which holds data by using a first clock, ... a Jth holding circuit which holds data by using a Jth clock (where: 1 < J < N), ... and an Nth holding circuit which holds data by using an Nth clock;

the first to Nth holding circuits are disposed along a line parallel to the lines of the first to Nth clocks;

the lines of the first to Nth clocks are connected to inputs of the first to Nth holding circuits, after being looped back in the opposite direction at first to Nth loop-back points; and

the first to Nth loop-back points are provided at positions such that the parasite capacitances of the lines of the first to Nth clocks are equal.

14. The clock generation circuit as defined in claim 8,

wherein the edge detection circuit comprises:

a first holding circuit which holds data by using a first clock, ... a Jth holding circuit which holds data by using a Jth clock (where: 1 < J < N), ... and an Nth holding circuit which holds data by using an Nth clock; and

a first detection circuit which detects whether or not there is a data edge between the edges of the first clock and a second clock, based on data held in the first holding circuit and a second holding circuit, ... a Jth detection circuit which detects whether or not there is a data edge between the edges of the Jth clock and a (J+1)th clock, based on data held in the Jth holding circuit and a (J+1)th holding circuit, ... and an Nth detection circuit which detects whether or not there is a

data edge between the edges of the Nth clock and the first clock, based on data held in the Nth holding circuit and the first holding circuit; and

wherein the clock selection circuit selects a clock from among the first to Nth clocks, based on edge detection information from the first to Nth detection circuits, and outputs the selected clock as the sampling clock.

15. The clock generation circuit as defined in claim 9,

wherein the edge detection circuit comprises:

a first holding circuit which holds data by using a first clock,... a Jth holding circuit which holds data by using a Jth clock (where: 1 < J < N),... and an Nth holding circuit which holds data by using an Nth clock; and

a first detection circuit which detects whether or not there is a data edge between the edges of the first clock and a second clock, based on data held in the first holding circuit and a second holding circuit,... a Jth detection circuit which detects whether or not there is a data edge between the edges of the Jth clock and a (J+1)th clock, based on data held in the Jth holding circuit and a (J+1)th holding circuit,... and an Nth detection circuit which detects whether or not there is a data edge between the edges of the Nth clock and the first clock, based on data held in the Nth holding circuit and the first holding circuit, and

wherein the clock selection circuit selects a clock from among the first to Nth clocks, based on edge detection

information from the first to Nth detection circuits, and outputs the selected clock as the sampling clock.

16. The clock generation circuit as defined in claim 14, wherein:

when a set-up time of the first to Nth holding circuits is TS, a hold time of the first to Nth holding circuits is TH, and a period of each of the first to Nth clocks is T, the number of clocks N of the first to Nth clocks is given by: $N \leqq [T/(TS + TH)]$ (where [X] is the maximum integer that does not exceed X).

17. The clock generation circuit as defined in claim 15, wherein:

when a set-up time of the first to Nth holding circuits is TS, a hold time of the first to Nth holding circuits is TH, and a period of each of the first to Nth clocks is T, the number of clocks N of the first to Nth clocks is given by: $N \leqq [T/(TS + TH)]$ (where [X] is the maximum integer that does not exceed X).

18. The clock generation circuit as defined in claim 16,

wherein the number of clocks N is defined by $N = [T/(TS + TH)]$ (where [X] is the maximum integer that does not exceed X).

19. The clock generation circuit as defined in claim 17,

wherein the number of clocks N is defined by N = [T/(TS + TH)] (where [X] is the maximum integer that does not exceed X).

20. The clock generation circuit as defined in claim 14, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

21. The clock generation circuit as defined in claim 15, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

22. The clock generation circuit as defined in claim 16, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

23. The clock generation circuit as defined in claim 17, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

24. The clock generation circuit as defined in claim 18, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

25. The clock generation circuit as defined in claim 19, wherein the number of clocks N of the first to Nth clocks is such that N = 5.

26. The clock generation circuit as defined in claim 8,

wherein the clock selection circuit selects a clock having an edge that is shifted by a given set number M of edges from a data edge, from among the first to Nth clocks, and outputs the selected clock as the sampling clock.

27. The clock generation circuit as defined in claim 9, wherein:

wherein the clock selection circuit selects a clock having an edge that is shifted by a given set number M of edges from a data edge, from among the first to Nth clocks, and outputs the selected clock as the sampling clock.

28. The clock generation circuit as defined in claim 26,

wherein the number M is set to a number that ensures set-up and hold times of a circuit which holds data based on the generated sampling clock.

29. The clock generation circuit as defined in claim 27,

wherein the number M is set to a number that ensures set-up and hold times of a circuit which holds data based on the generated sampling clock.

30. A data transfer control device for transferring data over a bus, the data transfer control device comprising:

the clock generation circuit as defined in claim 1; and

a circuit which holds data based on a sampling clock generated by the clock generation circuit, and performs given processing for data transfer, based on the held data.

31. A data transfer control device for transferring data over a bus, the data transfer control device comprising:

the clock generation circuit as defined in claim 7; and

a circuit which holds data based on a sampling clock generated by the clock generation circuit, and performs given processing for data transfer, based on the held data.

32. A data transfer control device for transferring data over a bus, the data transfer control device comprising:

the clock generation circuit as defined in claim 8; and

a circuit which holds data based on a sampling clock generated by the clock generation circuit, and performs given processing for data transfer, based on the held data.

33. A data transfer control device for transferring data over a bus, the data transfer control device comprising:

the clock generation circuit as defined in claim 9; and

a circuit which holds data based on a sampling clock generated by the clock generation circuit, and performs given processing for data transfer, based on the held data.

34. The data transfer control device as defined in claim 30, wherein data transfer is in accordance with the universal

serial bus (USB) standard.

35. The data transfer control device as defined in claim 31, wherein data transfer is in accordance with the universal serial bus (USB) standard.

36. The data transfer control device as defined in claim 32, wherein data transfer is in accordance with the universal serial bus (USB) standard.

37. The data transfer control device as defined in claim 33, wherein data transfer is in accordance with the universal serial bus (USB) standard.

38. An electronic instrument comprising:

the data transfer control device as defined in claim 30; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

39. An electronic instrument comprising:

the data transfer control device as defined in claim 31; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

40. An electronic instrument comprising:

the data transfer control device as defined in claim 32; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

41. An electronic instrument comprising:

the data transfer control device as defined in claim 33; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

42. An electronic instrument comprising:

the data transfer control device as defined in claim 34; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

43. An electronic instrument comprising:

the data transfer control device as defined in claim 35; and

a device which performs output processing, fetch processing or storage processing on data transferred through

the data transfer control device and the bus.

44. An electronic instrument comprising:

the data transfer control device as defined in claim 36; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.

45. An electronic instrument comprising:

the data transfer control device as defined in claim 37; and

a device which performs output processing, fetch processing or storage processing on data transferred through the data transfer control device and the bus.